REMARKS

ALLOWABLE SUBJECT MATTER

Claims 3-7 and 10-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

REJECTION UNDER 35 U.S.C.§102

A. Claims 1-2 and 8-9 are rejected under 35 U.S.C. §102(b) as being anticipated by Ohara (USPN 5,517,132).

In general, the present invention relates to a method and an apparatus for obtaining an RTL model which is suitable for formal verification by processing a conventional RTL specification to obtain a reduced RTL specification, i.e., an RTL specification wherein the widths of the signals are reduced. Examples are found on pages 8-10 of the specification of the present application.

Consequently, the object underlying the present invention is to provide an RTL specification better suitable for formal verification.

In contrast, Ohara relates to a method for generating a semiconductor integrated circuit from data of register-transfer level, i.e., from an RTL description. In particular, it addresses the problem that the power consumption of a semiconductor circuit is dependent on the supply voltage, and it is thus desirable to choose a supply voltage that is as low as possible. However, some parts of the circuit, called "critical paths" by Ohara, have to be driven by a high voltage (see, e.g., col. 1, line 63 to col. 2, line 7). Since this critical path has to communicate with the rest of the circuit, so-called level converters have to be provided between elements operating at a low voltage and elements operating at a high voltage (see col.2, lines 8 to 12). As those level converters consume chip space and are difficult to place, Ohara provides a method for generating a semiconductor integrated circuit with a reduced number of level converters by optimizing interconnects and by integrating level converters within registers (see col. 2, line 51 to col. 3, line 40). However, reducing the number of level converters corresponds to a reduction of

the number of hardware elements needed and has nothing to do with the reduction of a signal width used in the present invention to derive a reduced RTL model from a "standard" RTL model. Also, the level conversion itself does not reduce a width of a signal, but changes the voltage levels used for representing the states of the signal.

Hence, it is respectfully submitted that Ohara neither discloses nor suggests the teaching of independent claims 1 and 8 of the present patent application. Thus, independent claims 1 and 8 are submitted to be allowable under 35 U.S.C. §102(b) and not anticipated by Ohara (USPN 5,517,132). Since claims 2 and 9 depend from claims 1 and 8, respectively, claims 2 and 9 are submitted to be allowable under 35 U.S.C. §102(b) and not anticipated by Ohara (USPN 5,517,132) for at least the reasons that claims 1 and 8 are submitted to be allowable.

B. Claims 1 and 8 are rejected under 35 U.S.C. §102(e) as being anticipated by Takemura et al.(USPN 6,523,153).

It is respectfully submitted that the Takamura et al. reference does not relate to a method and to an apparatus for obtaining a reduced RTL model from an RTL model. Takemura et al. refers to the situation in which part of a system (i.e., a circuit) is described by a behavioral model and part of the system is described by an RTL model (see col. 1, lines 57-67). The problem connected therewith is that it is not possible to verify the overall system because of the different descriptions of various parts of the system. Therefore, as described in the abstract, Takamura et al. discloses a method to generate an interface model for communication between a behavioral model and an RTL model so that, with the help of such interface modules, the overall system may be verified. While it is true that, within this interface model, a signal may be converted from one bit width to another (see col. 8, lines 5 to 10), this is done because the behavioral model may use a different signal representation than the RTL model. Thus, this is just a conversion so that the two models can communicate with one another (see, e.g., FIG. 2A and FIG. 2B) and not to derive a reduced RTL model from a standard RTL model.

It should be noted that the present invention may be used in the step of verifying the RTL model description mentioned in column 1, line 60/61 of Takemura et al. for obtaining an RTL model which may be verified with less effort.

Thus, it is respectfully submitted that claims 1 and 8 are allowable under 35 U.S.C. §102(e) and are not anticipated by Takemura et al.(USPN 6,523,153).

C. Claims 1-2 and 8-9 are rejected under 35 U.S.C. §102(b) as being anticipated by Sharma et al. (USPN 5,841,663).

It is respectfully submitted that Sharma et al. also does not refer to a method for deriving a reduced RTL model from a standard RTL model by reducing signal widths. The terminology in col. 7, lines 51-53 to which the Examiner refers in the Office Action describes that data paths are partitioned based upon the signal width, i.e., expressions with the same widths are groups and assigned to group data paths having the required width. This means that the actual width of the expression is not changed. In contrast, the purpose of this step, since the aim of Sharma et al. is to provide an actual net list, is to use common data paths for signals of the same signal width so that no data paths which are designed for a greater signal width than the signal actually transmitted over this data path have to be used.

Hence, it is respectfully submitted that Sharma et al. does not suggest or disclose the subject matter of the present independent claims (1 and 8) of the present patent application.

Thus, independent claims 1 and 8 are submitted to be allowable under 35 U.S.C. §102(b) and not anticipated by Sharma et al. (USPN 5,841,663). Since claims 2 and 9 depend from claims 1 and 8, respectively, claims 2 and 9 are submitted to be allowable under 35 U.S.C. §102(b) and not anticipated by Sharma et al. (USPN 5,841,663) for at least the reasons that claims 1 and 8 are submitted to be allowable.

CONCLUSION

In accordance with the foregoing, a response has been presented which respectfully explains that it is the applicant's position that the prior art references referred to by the Examiner with respect to the subject matter of the present independent claims 1 and 8 do not relate to obtaining a reduced RTL model form an existing RTL model, the reduced RTL model having a signal width smaller than the signal width of the existing RTL model, thus indicating that the subject matter of the independent claims is neither disclosed nor rendered obvious by the cited prior art references. Hence, the claims have not been amended. Dependent claims 2-7 and 9-13, which depend from independent claims 1 and 8, respectively, are submitted to be allowable for at least the reasons that claims 1 and 8 are submitted to be allowable.

Claims 1-13 are pending and under consideration.

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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Date: November 20, 2003

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